**Lab 3: Decoders, Displays & Multiplexers**

**ITI 1100 C – Digital Systems 1**

**Winter 2016**

**School of Electrical Engineering and Computer Science**

**University of Ottawa**

**Course Coordinator: Dr. Ahmed Karmouch**

**Teaching Assistants:**

Group #: 26

Student Name and Number: Abigail Woods, 7619696

Student Name and Number: Felix Singerman, 7970742

Experiment Date: 2016-03-01

Submission Date: 2016-03-15

**Lab 3: Decoders, Displays & Multiplexers**

**Objectives**

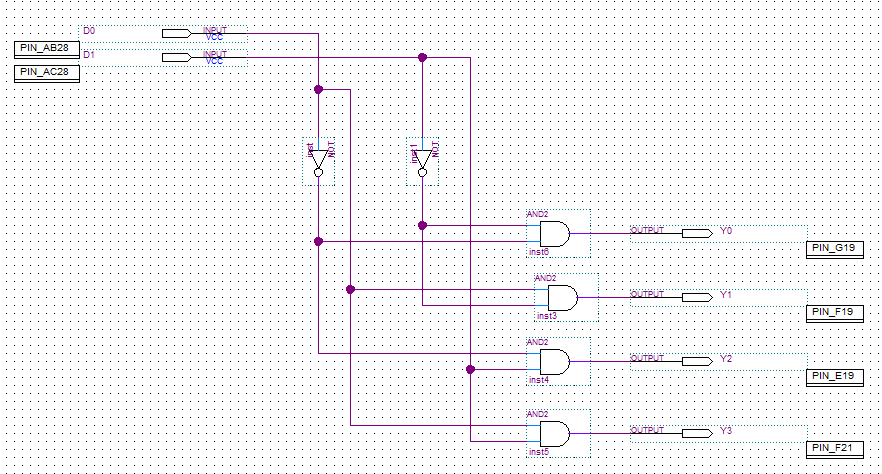
* Analyse, construct and test a simple 2-to-4 decoder
* Construct and test a seven-segment decoder display
* Analyse, construct and test a simple multiplexer

**Equipment and Components**

* Quartus II 13.0 Service-Pack 1 Software (64-bit)
* Altera DE2-115 circuit board
* Altera DE2-115 chip (EP4CE115F29C7N)

**Circuit Diagrams**

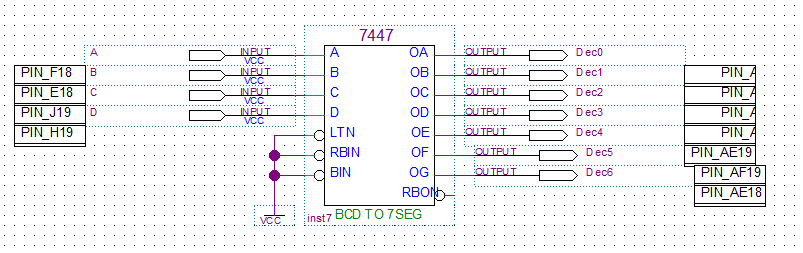
**Part 1 – A 2-to-4 Decoder**

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**Figure 1.1:** Screen-shot of a 2-to-4 decoder circuit.

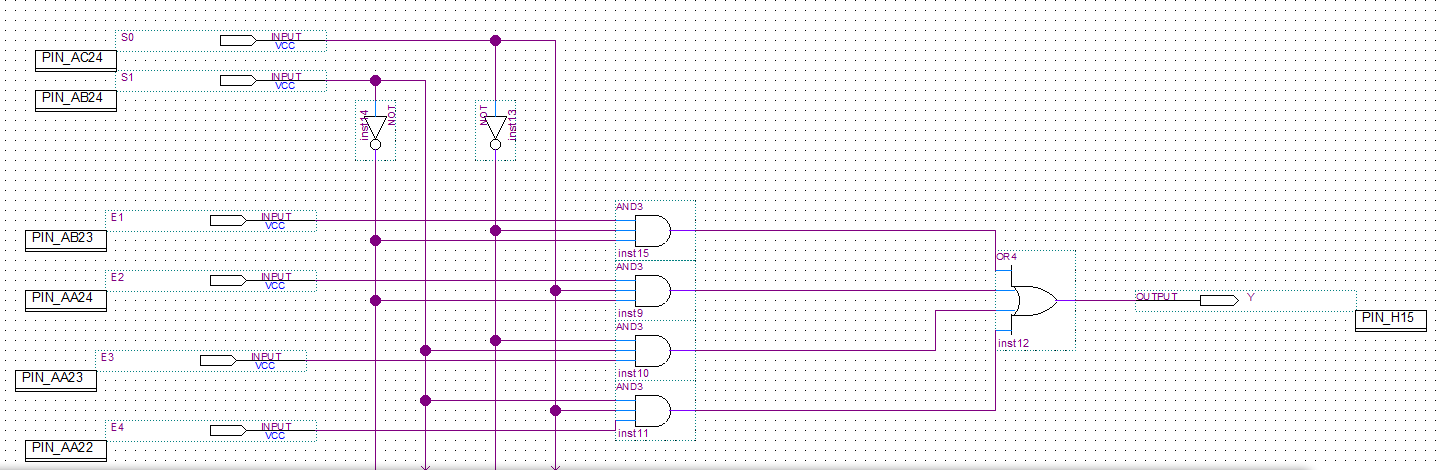
**Part II – Decoder and**

**Seven-Segment Display**

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**Figure 2.1:** Screen-shot of the combinational decoder and seven segment display diagram.

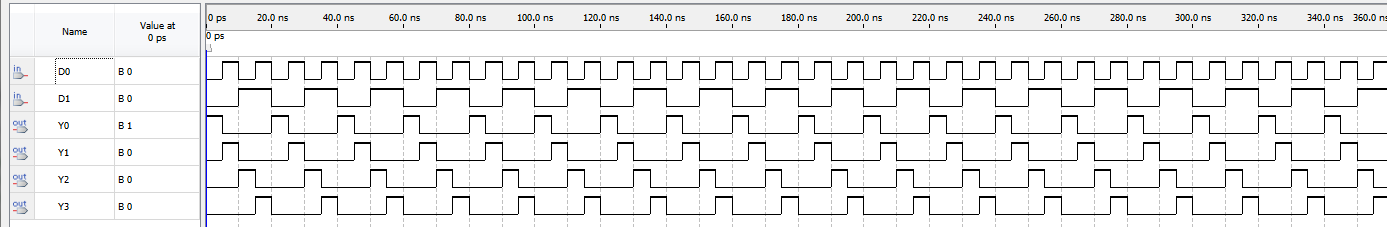
**Part III – Multiplexers**



**Figure 3.1:** Screen-shot of the multiplexer diagram.

**Experimental Data and Data Processing**

**Part 1 – A 2-to-4 Decoder**



**Figure 1.2:** Screen-shot of the simulation output of the 2-to-4 decoder.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Given Input** | | **Observed Output** | | | |
| **D0** | **D1** | **Y0** | **Y1** | **Y2** | **Y3** |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

**Table 1.3:** Truth table for the 2-to-4 decoder.

**Part II – Decoder and Seven-Segment Display**

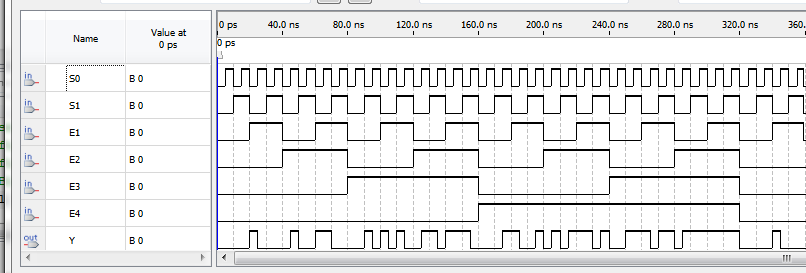
|  |  |
| --- | --- |
| **D3D2D1D0** | **Corresponding Display** |
| 0000 | 0 |
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |

**Table 2.3:** Truth table for the decoder and seven-segment display.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Given Input** | | | | **Observed Output** | | | | | | |
| **D** | **C** | **B** | **A** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | x | x | **X** | x | x | x | **X** |
| 1 | 0 | 1 | 1 | x | x | x | x | **X** | x | x |
| 1 | 1 | 0 | 0 | x | x | x | x | x | x | **X** |
| 1 | 1 | 0 | 1 | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | **X** |
| 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |

**Table 2.4:** Truth table for the decoder and seven-segment display.

**Part III – Multiplexers**



**Figure 3.2:** Screen-shot of the simulation output of the multiplexers.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Input Given** | | | | | | **Observed Output** |
| **S0** | **S1** | **D0** | **D1** | **D2** | **D3** | **Y** |
| 0 | 0 | 1 | X | X | X | 1 |
| 0 | 1 | X | 1 | X | X | 1 |
| 1 | 0 | X | X | 1 | X | 1 |
| 1 | 1 | X | X | X | 1 | 1 |
| 0 | 0 | 0 | X | X | X | 0 |
| 0 | 1 | X | 0 | X | X | 0 |
| 1 | 0 | X | X | 0 | X | 0 |
| 1 | 1 | X | X | X | 0 | 0 |

**Table 3.3:** Truth table for the multiplexer.

**Comparison of Theoretical Data and Experimental Data**

**Part 1 – A 2-to-4 Decoder**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input Given** | | **Observed Results** | | | | **Expected Results** | | | |
| **A** | **B** | **Y0** | **Y1** | **Y2** | **Y3** | **D0** | **D1** | **Y0** | **Y1** |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**Table 1.4:** Comparison of the theoretical and experimental results for the 2-to-4 decoder.

The results obtained experimentally from the circuit board were identical to the theoretical results computed. This adheres to the laws of Boolean logic and algebra.

**Part II – A Decoder and Seven Segment Display**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Given Input** | | | | **Observed Results** | | | | | | | **Expected Results** | | | | | | |
| **D** | **C** | **B** | **A** | **a** | **b** | **c** | **d** | **e** | **f** | **g** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | x | x | **X** | x | x | x | **X** | x | x | **X** | x | x | x | **X** |
| 1 | 0 | 1 | 1 | x | x | x | x | **X** | x | x | x | x | x | x | **X** | x | x |
| 1 | 1 | 0 | 0 | x | x | x | x | x | x | **X** | x | x | x | x | x | x | **X** |
| 1 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| 1 | 1 | 1 | 0 | x | x | x | x | x | x | **X** | x | x | x | x | x | x | **X** |
| 1 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | x | x | x | x | x |

**Table 2.4:** Comparison of the theoretical and experimental results for a decoder and seven-segment display.

The results obtained experimentally from the circuit board were identical to the theoretical results computed. 10 (#’s 0-9) sets of inputs generated unique and proper number outputs on the LED display. 6 sets of inputs however were irrelevant and do not generate specific outputs.

**Part III – Multiplexers**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Input Given** | | | | | | **Observed Results** | **Expected Results** |
| **S0** | **S1** | **D0** | **D1** | **D2** | **D3** | **Y** | **Y** |
| 0 | 0 | 1 | X | X | X | 1 | 1 |
| 0 | 1 | X | 1 | X | X | 1 | 1 |
| 1 | 0 | X | X | 1 | X | 1 | 1 |
| 1 | 1 | X | X | X | 1 | 1 | 1 |
| 0 | 0 | 0 | X | X | X | 0 | 0 |
| 0 | 1 | X | 0 | X | X | 0 | 0 |
| 1 | 0 | X | X | 0 | X | 0 | 0 |
| 1 | 1 | X | X | X | 0 | 0 | 0 |

**Table 3.4:** Comparison of the theoretical and experimental results of the multiplexer.

The results obtained experimentally with the Multiplexer were identical to those computed theoretically. This indicates that even when data inputs are used, circuits must adhere to the same logics of Boolean algebra.

**Discussion and Conclusions**

The objective of this experiment was to construct and test a simple 2-to-4 decoder, a seven-segment decoder display and a simple multiplexer. For this lab all of the experimental results once again matched the computed theoretical results. This is due to logic circuits adhering to the laws of Boolean algebra and logic. With the BCD decoder it was shown how in a logic circuit certain combinations of inputs are not relevant to the desired output. This is what leads to don’t care conditions. With the multiplexer, the effect of data-inputs on a circuit was illustrated. A circuit with data inputs sill follows the same laws of Boolean logic as one without them.

**Appendix (Pre-Lab)**

See the following pages for the pre-lab predictions written for this lab.